Roll No. | | | | | | | | | | |

ANNA UNIVERSITY (UNIVERSITY DEPARTMENTS)

B.E. / B. Tech / B. Arch (Full Time) - END SEMESTER EXAMINATIONS, APRIL / MAY 2024

INFORMATION TECHNOLOGY
Semester 4
IT5451 Computer Architecture
(Regulation 2019)

Time: 3hrs

Max.Marks: 100

CO 1	Interpret assembly language instructions.
CO 2	Design and analyze ALU circuits.
CO 3	Implement a control unit as per the functional specification.
CO 4	Design and analyze memory, I/O devices and cache structures for processor.
CO 5	Evaluate the performance of computer systems
CO 6	Point out the hazards present in a pipeline and suggest remedies

BL – Bloom's Taxonomy Levels
(L1 - Remembering, L2 - Understanding, L3 - Applying, L4 - Analysing, L5 - Evaluating, L6 - Creating)

PART- A (10 x 2 = 20 Marks)
(Answer all Questions)

Q. No	Questions	Marks	CO	BL
1	How does the instruction set architecture affect CPU Performance?	2	1	2
2	How has Moore's law impacted the semiconductor industry?	2	2	2
3	Show the IEEE 754 binary representation of -0.75 in double precision.	2	2	3
4	Convert the following 'C' statement to MIPS assemble code? R = a + (b -10);	2	1	3
5	What are the main stages of executing an instruction in a processor?	2	4	1
6	What is the need for inter-stage registers in a pipelined architecture?	2	5	2
7	Determine the number of virtual pages, the bits used for the virtual page number and the page offset for 1 GB page size in a 32-bit ISA.	2	4	4
8	What is the difference between a pipeline bubble and NOP(No operation)?	2	6	5
9	What are some common applications of GPUs beyond graphics rendering?	2	5	2
10	How will next-generation processors handle the increasing demand for AI and machine learning applications?	2	5	3

PART- B (5 x 13 = 65 Marks)

Q. No	Questions	Marks	CO	BL
11 (a) (i)	The Fibonacci Sequence is the series of numbers: 0, 1, 1, 2, 3, 5, 8, 13, 21, 34,.. Any number in the series is found by adding up the two numbers before it. Write a MIPS program to perform the following: Given a positive integer $0 \le n \le 20$, store the first n numbers of the Fibonacci series in memory and print them	7	1	3
(ii)	How does Amdahl's law illustrate the diminishing returns of adding more processors? Give an example demonstrating Amdahl's law.	6	5	2

	OR			
11 (b) (i)	Write short notes on different types of MIPS addressing modes with an example.	**5**	1	1
(ii)	Assume a program requires the execution of 50×10^6 FP instructions, 110×10^6 INT instructions, 80×10^6 Load/Store instructions, and 16×10^6 branch instructions. The CPI for each type of instruction is 1, 1, 4, and 2, respectively. Assume that the processor has a 2 GHz clock rate. a) By how much must we improve the CPI of FP instructions if we want the program to run two times faster? b) By how much must we improve the CPI of L/S instructions if we want the program to run two times faster? c) By how much is the execution time of the program improved if the CPI of INT and FP instructions is reduced by 40% and the CPI of L/S and Branch is reduced by 30%	 **2** **3** **3**	5	5
12 (a) (i)	Draw the hardware arrangement required for carry – save addition of summands and perform both bit – pair recoding of multipliers and carry – save addition of summands of A and B where A=011011 (Multiplicand) and B=110101 (Multiplier). Show the content of registers after each step.	**13**	2	3
	OR			
12 (b) (i)	Compute the Booth multiplication of A and B where $A = -7$ (Multiplicand) and $B = -15$ (Multiplier).	**5**	2	5
(ii)	Compare and contrast restoring and non -restoring division. Using the restoring division algorithm find the result of the following division 133/7	**8**	2	5
13 (a) (i)	What are the different types of hazards that might arise in a pipeline? Point out ways of handling them.	**5**	6	3
(ii)	Draw and explain the full data-path in a MIPS single cycle pipeline showing the control signals that need to be generated to execute the instruction: sw $s0, 5($s1)	**8**	4	5
	OR			
13 (b) (i)	Find the data dependencies between all the instructions below. I1. sub R2, R5, R4 I2. add R4, R2, R5 I3. lw R5, 100(R2) I4. sub R2, R5, R4 I5. sw R2, 101(R2)	**5**	6	4

(ii)	How long will the following code take on a 5-stage MIPS pipeline with forwarding and appropriate NOPs? Fill out the pipeline and draw the forwarding path in the pipeline. How many cycles it takes to execute all three instructions?
	add R5, R5, R7
	lw R6, 100(R7)
	sub R7, R6, R8
		8	3	5

14 (a) (i)	A processor has a 32-bit memory address space. The memory is broken into blocks of 32 bytes. The computer has a cache capable of storing 16K bytes a. How many blocks can the cache store? b. Assume the cache uses direct-mapping, how many bits are there in each of the TAG, BLOCK, and BYTE OFFSET fields of the address. Show your calculations. c. Assuming the cache uses a 4-way set-associative mapping, how many bits are there in each of the TAG,SET and BYTE OFFSET fields of the address.	 **3** **3** **3**	4	3

(ii)	Describe the primary components of a DMA controller and their functions.	**4**	4	1
	OR			
14(b) (i)	Explain the relationship between the TLB and the CPU cache. How do they complement each other in a memory hierarchy?	**7**	4	3
(ii)	Consider a virtual memory system with the following properties: 40-bit virtual byte address, 16 KB pages, 36-bit physical byte address. TLB has 8 entries and fully associative. Valid, protection, dirty and use bits take a total of 4 bits (both TLB and page table have these). Compute: a. Total size (in bits) of TLB b. The Total size (in bits) of page table	 **3** **3**		
15 (a) (i)	Provide a step-by-step example of how Tomasulo's Algorithm schedules and executes instructions, including the reservation stations, functional units, and result forwarding for the given instructions. Assume there are 2 loaders, 2 adders, 2 multipliers and at each cycle one instruction is dispatched. Schedule the following code L.D F6,34(R2) L.D F2,45(R3) MUL.D F0, F2, F4 SUB.D F8, F2, F6 DIV.D F10, F0, F6 ADD.D F6, F8, F2 The following are the latencies: ADD 2, MULT 10, DIV 40	**13**	6	3
	OR			
15 (b) (i)	Explain the concept of multicore processors, where multiple processing cores are integrated onto a single chip. Contrast this with single-core processors, which have only one processing unit and highlight the benefits of multicore processors in terms of parallelism and performance.	**13**	5	2

PART- C (1 x 15 = 15 Marks)

(Q.No.16 is compulsory)

Q. No	Questions	Marks	CO	BL
16. (i)	Write a MIPS function sum_digits that computes and returns the sum of decimal digits in an unsigned integer. For example, the sum of decimal digits for 1536 is 1+5+3+6 = 15. The function sum_digits receives the unsigned integer argument in binary in register $a0. For example, 1536 = (0000 … 0110 0000 0000) binary. It should extract the decimal digits, compute, and return their sum, also in binary, in register $v0. Hint: divide the unsigned integer by 10 to extract the decimal digits.	**8**	1	6
(ii)	Determine the g_i , p_i ,P_i and G_i values of these two 16-bit numbers: a: 0001 1010 0011 0011 b: 1110 0101 1110 1011 Also, what is the CarryOut15(C4)?	**7**	2	3